



**Model Name:GA-970A-D3**

### Component value change history

**Version: 1.02**

P-Code: U98094-0

[illegible]

### Circuit or PCB layout change for next version

[illegible]**GIGABYTE™**

Title

## BOM & PCB HISTORY

Size	1
Custom	

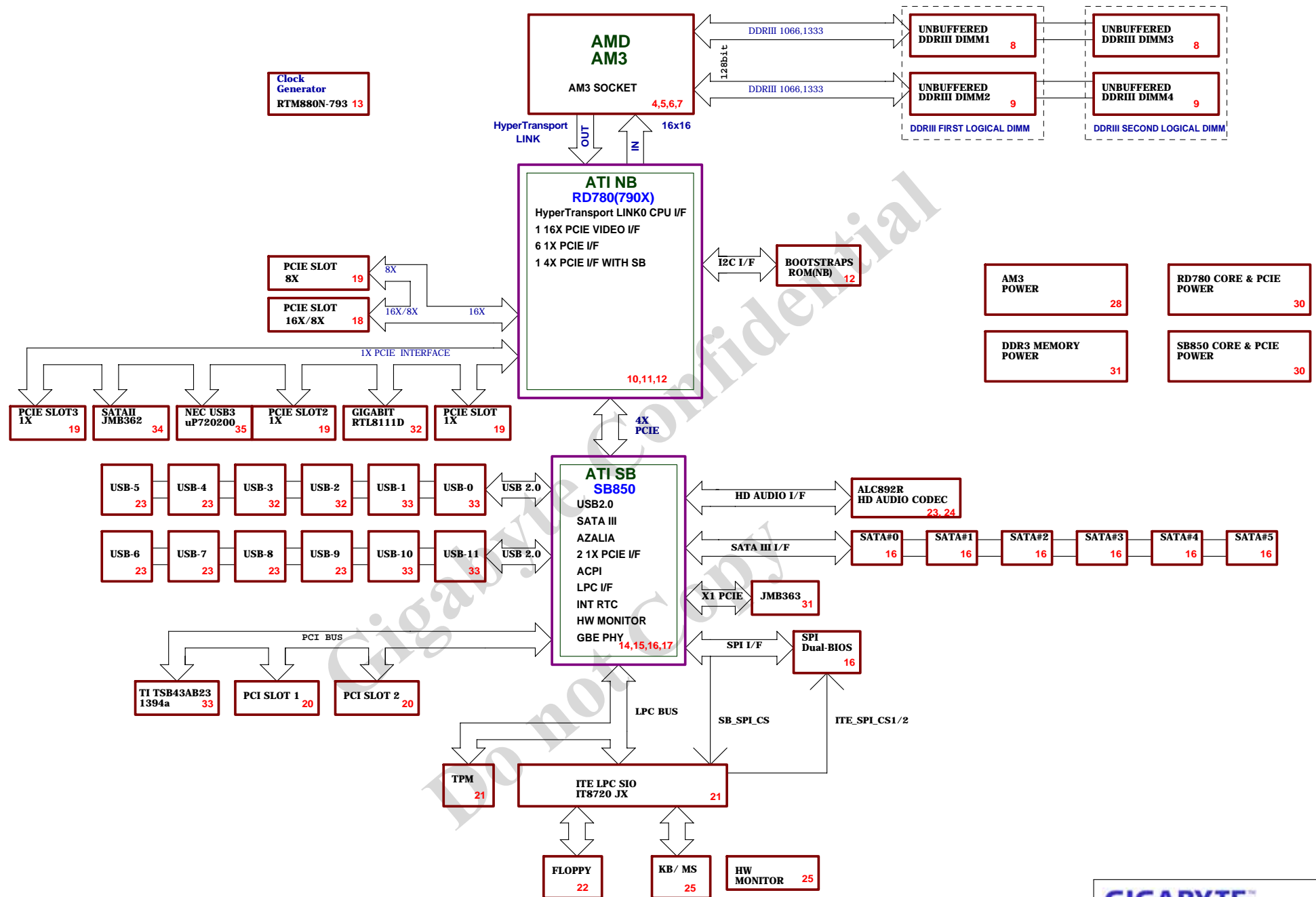
Document Number	
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GA-970A-D3

Rev	1.02
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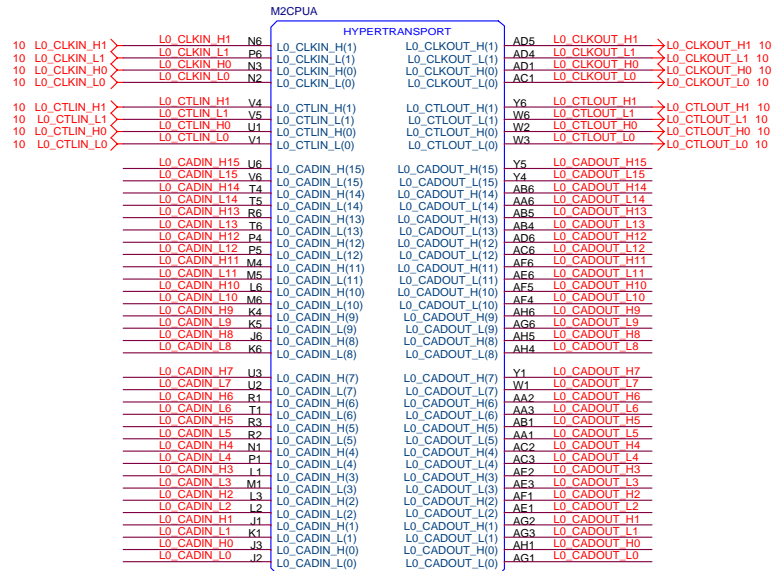
Date: Tuesday, June 28, 2011

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**GIGABYTE**

Title			BLOCK DIAGRAM	
Size	Document Number			Rev
Custom	GA-970A-D3			1.02
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L0\_CADIN\_L[0..15] < L0\_CADIN\_L[0..15] 10  
 L0\_CADIN\_H[0..15] < L0\_CADIN\_H[0..15] 10  
 L0\_CADOUT\_L[0..15] < L0\_CADOUT\_L[0..15] 10  
 L0\_CADOUT\_H[0..15] < L0\_CADOUT\_H[0..15] 10

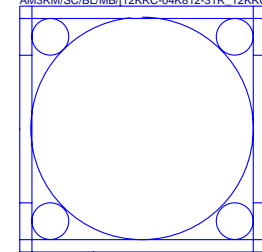


CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR15V  
 CPU\_VDDR = CPU\_VDDR12

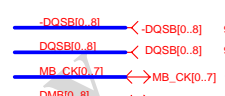
VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B



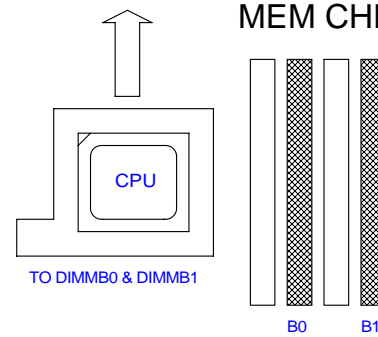
M2CPU  
 AM3RM/SC/BL/MB/(12KRC-04K812-31R\_12KRC-04K812-32R)



GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
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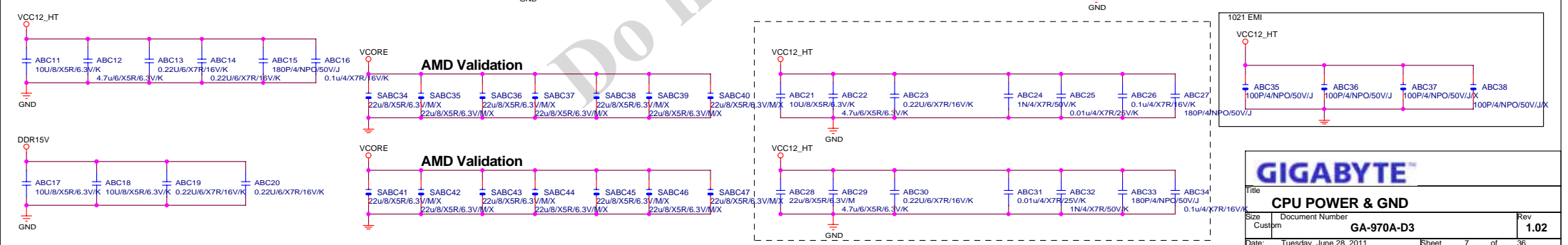
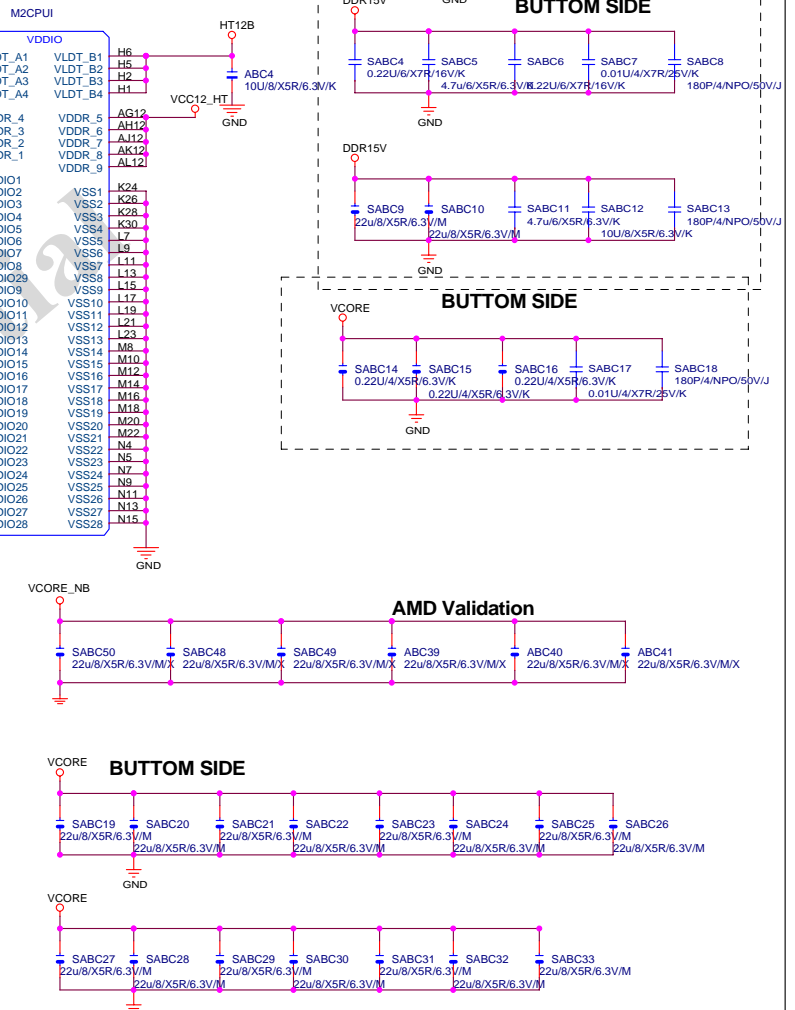
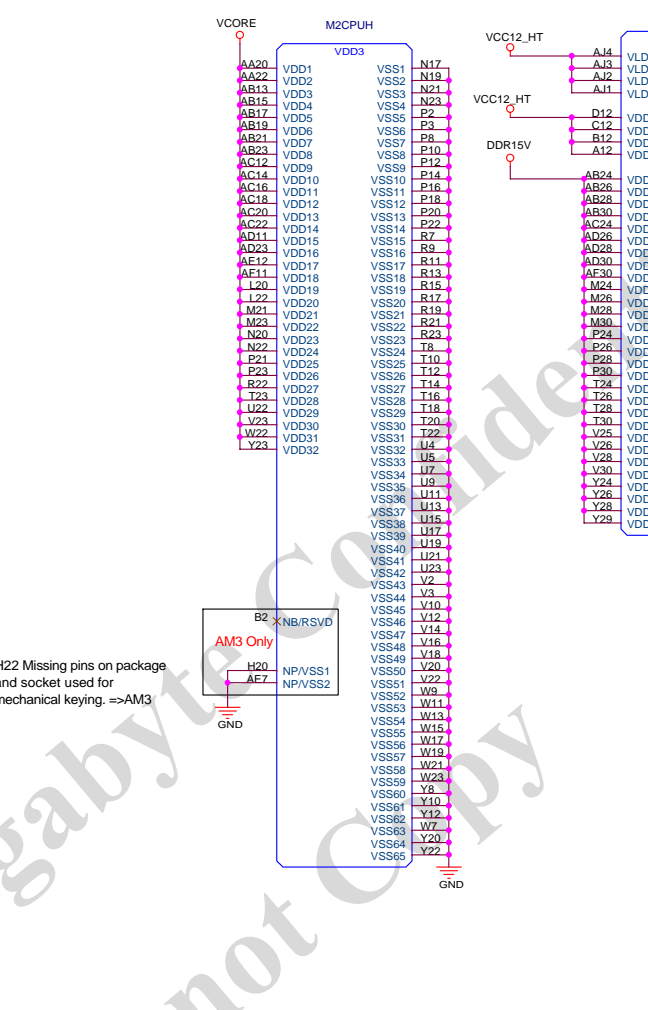


MEM CHB

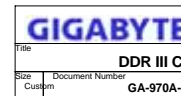
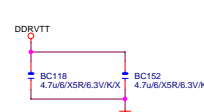
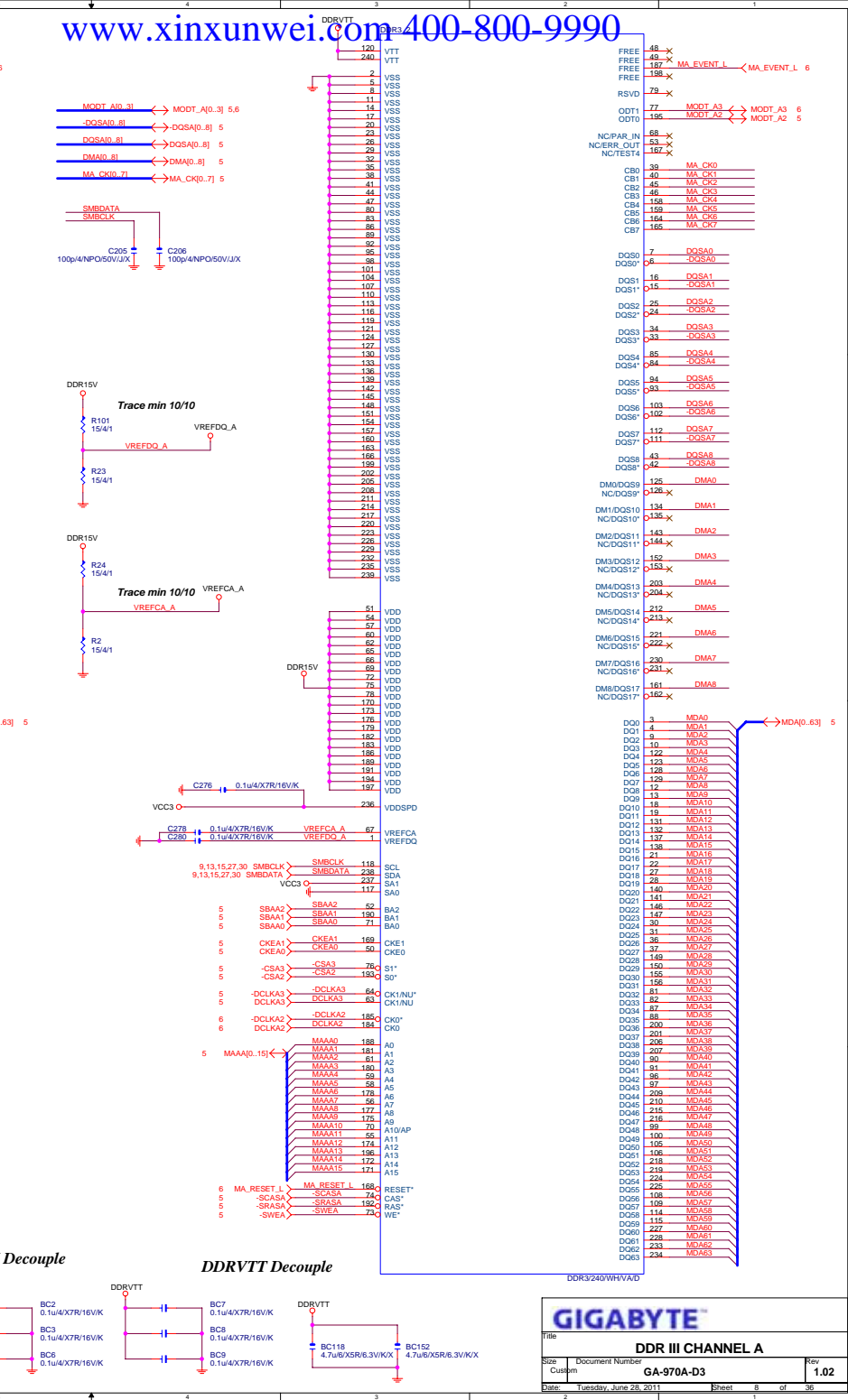


				
Title <b>CPU DDRIII MEMORY</b>				
Size	Document Number			Rev
Custom	<b>GA-970A-D3</b>			<b>1.02</b>
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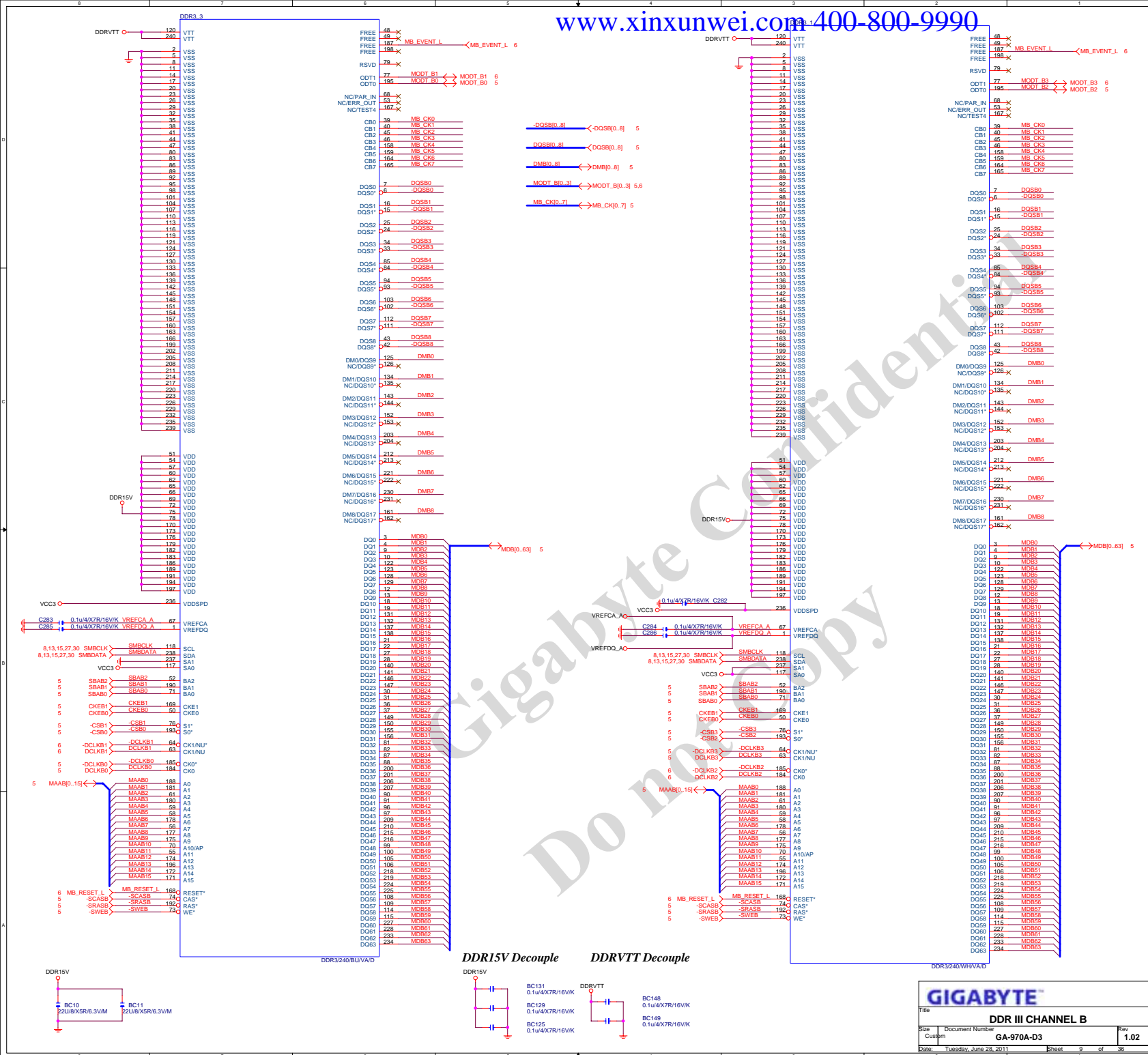












U3A

## PART 1/5

HYPERTRANSPORT  
IF

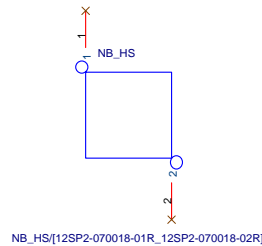
RX980/BGA692

L0\_CADIN\_L[0..15] &lt;L0\_CADIN\_L[0..15] 4

L0\_CADIN\_H[0..15] &lt;L0\_CADIN\_H[0..15] 4

L0\_CADOUT\_L[0..15] &lt;L0\_CADOUT\_L[0..15] 4

L0\_CADOUT\_H[0..15] &lt;L0\_CADOUT\_H[0..15] 4

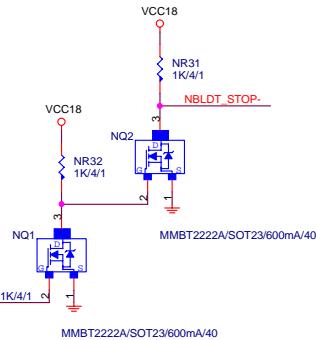


HT_TXCAD15P	N23	L0_CADIN_H15
HT_TXCAD15N	N24	L0_CADIN_L15
HT_TXCAD14P	M24	L0_CADIN_H14
HT_TXCAD14N	M25	L0_CADIN_L14
HT_TXCAD13P	L23	L0_CADIN_H13
HT_TXCAD13N	L24	L0_CADIN_L13
HT_TXCAD12P	K24	L0_CADIN_H12
HT_TXCAD12N	K25	L0_CADIN_L12
HT_TXCAD11P	H24	L0_CADIN_H11
HT_TXCAD11N	H25	L0_CADIN_L11
HT_TXCAD10P	G24	L0_CADIN_H10
HT_TXCAD10N	G24	L0_CADIN_L10
HT_TXCAD9P	F24	L0_CADIN_H9
HT_TXCAD9N	F25	L0_CADIN_L9
HT_TXCAD8P	E24	L0_CADIN_H8
HT_TXCAD8N	E23	L0_CADIN_L8
HT_TXCAD7P	N26	L0_CADIN_H7
HT_TXCAD7N	N27	L0_CADIN_L7
HT_TXCAD6P	M27	L0_CADIN_H6
HT_TXCAD6N	M28	L0_CADIN_L6
HT_TXCAD5P	L26	L0_CADIN_H5
HT_TXCAD5N	L27	L0_CADIN_L5
HT_TXCAD4P	K27	L0_CADIN_H4
HT_TXCAD4N	K28	L0_CADIN_L4
HT_TXCAD3P	H27	L0_CADIN_H3
HT_TXCAD3N	H28	L0_CADIN_L3
HT_TXCAD2P	G27	L0_CADIN_H2
HT_TXCAD2N	G27	L0_CADIN_L2
HT_TXCAD1P	F27	L0_CADIN_H1
HT_TXCAD1N	F28	L0_CADIN_L1
HT_TXCAD0P	E26	L0_CADIN_H0
HT_TXCAD0N	E27	L0_CADIN_L0

HT_RXCLK1P	J23	L0_CLKIN_H1
HT_RXCLK1N	J24	L0_CLKIN_L1
HT_RXCLK0P	J26	L0_CLKIN_H0
HT_RXCLK0N	J27	L0_CLKIN_L0

HT_RXCTL1P	P24	L0_CTLIN_H1
HT_RXCTL1N	P25	L0_CTLIN_L1
HT_RXCTL0P	P27	L0_CTLIN_H0
HT_RXCTL0N	P28	L0_CTLIN_L0

HT_TXCALP	D28	HT_TXCALN
HT_TXCALN	D27	HT_TXCALN



U3C

PART 3/5  
CLOCKS

## PM

## MISC.

STRP\_DATA

TESTMODE

## DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEB

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using nbcfg register access)  
0 : Enable

## DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCIe GPP mode.  
GPIO4:3:2  
000 : 4:2:4 B  
001 : 4:1:1:4 C  
010 : 1:1:1:1:1:1:4 L (Hardware Default)  
011 : 2:1:1:1:1:4 E  
100 : 2:2:1:1:4 K  
101 : 2:2:2:4 C2  
110: Hardware default (mode L) or EEPROM  
111: Hardware default (mode L) or EEPROM  
101 : 01100  
111 : 01011

## DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

## DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEB

Enables the Test Debug Bus using PCIe bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

GIGABYTE®

Title RS780 HT-LINK I/F

Size Document Number  
Custom GA-970A-D3

Rev 1.02

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U3B

PART 2/5

EXP A_RXP15	N6	GPP1_RX15P	GPP1_TX15P	N3	EXP A_TXP15
EXP A_RXN15	N5	GPP1_RX15N	GPP1_TX15N	M2	EXP A_TXN15
EXP A_RXP14	M5	GPP1_RX14P	GPP1_TX14P	M1	EXP A_TXN14
EXP A_RXN14	M4	GPP1_RX14N	GPP1_TX14N	L3	EXP A_TXP13
EXP A_RXP13	L6	GPP1_RX13P	GPP1_TX13P	L2	EXP A_TXN13
EXP A_RXN13	L5	GPP1_RX13N	GPP1_TX13N	K2	EXP A_TXP12
EXP A_RXP12	K5	GPP1_RX12P	GPP1_TX12P	K1	EXP A_TXN12
EXP A_RXN12	K4	GPP1_RX12N	GPP1_TX12N	J3	EXP A_TXP11
EXP A_RXP11	J6	GPP1_RX11P	GPP1_TX11P	J2	EXP A_TXN11
EXP A_RXN11	J5	GPP1_RX11N	GPP1_TX11N	H2	EXP A_TXP10
EXP A_RXP10	H5	GPP1_RX10P	GPP1_TX10P	H1	EXP A_TXN10
EXP A_RXN10	H4	GPP1_RX10N	GPP1_TX10N	G3	EXP A_TXP9
EXP A_RXP9	G6	GPP1_RX9P	GPP1_TX9P	G2	EXP A_TXN9
EXP A_RXN9	G5	GPP1_RX9N	GPP1_TX9N	F2	EXP A_TXP8
EXP A_RXP8	F5	GPP1_RX8P	GPP1_TX8P	F1	EXP A_TXN8
EXP A_RXN8	F4	GPP1_RX8N	GPP1_TX8N	E3	EXP A_TXP7
EXP A_RXP7	D2	GPP1_RX7P	GPP1_TX7P	E2	EXP A_TXN7
EXP A_RXN7	D1	GPP1_RX7N	GPP1_TX7N	A4	EXP A_TXP6
EXP A_RXP6	B5	GPP1_RX6P	GPP1_TX6P	B4	EXP A_TXN6
EXP A_RXN6	C6	GPP1_RX6N	GPP1_TX6N	A6	EXP A_TXP5
EXP A_RXP5	D6	GPP1_RX5P	GPP1_TX5P	B6	EXP A_TXN5
EXP A_RXN5	E6	GPP1_RX5N	GPP1_TX5N	B7	EXP A_TXP4
EXP A_RXP4	E7	GPP1_RX4P	GPP1_TX4P	C7	EXP A_TXN4
EXP A_RXN4	F7	GPP1_RX4N	GPP1_TX4N	A8	EXP A_TXP3
EXP A_RXP3	D8	GPP1_RX3P	GPP1_TX3P	B8	EXP A_TXN3
EXP A_RXN3	E8	GPP1_RX3N	GPP1_TX3N	B9	EXP A_TXP2
EXP A_RXP2	E9	GPP1_RX2P	GPP1_TX2P	C9	EXP A_TXN2
EXP A_RXN2	F9	GPP1_RX2N	GPP1_TX2N	A10	EXP A_TXP1
EXP A_RXP1	D10	GPP1_RX1P	GPP1_TX1P	B10	EXP A_TXN1
EXP A_RXN1	E10	GPP1_RX1N	GPP1_TX1N	B11	EXP A_TXP0
EXP A_RXP0	E11	GPP1_RX0P	GPP1_TX0P	C11	EXP A_TXN0
EXP A_RXN0	F11	GPP1_RX0N	GPP1_TX0N		

AC9	GPP2_RX15P	GPP2_TX15P	AF9
AD9	GPP2_RX15N	GPP2_TX15N	AG9
AE8	GPP2_RX14P	GPP2_TX14P	AG8
AE7	GPP2_RX14N	GPP2_TX14N	AH8
AC7	GPP2_RX13P	GPP2_TX13P	AF7
AD7	GPP2_RX13N	GPP2_TX13N	AG7
AD6	GPP2_RX12P	GPP2_TX12P	AG6
AE6	GPP2_RX12N	GPP2_TX12N	AH6
AE5	GPP2_RX11P	GPP2_TX11P	AG4
AG5	GPP2_RX11N	GPP2_TX11N	AH4
AE2	GPP2_RX10P	GPP2_TX10P	AE3
AF1	GPP2_RX10N	GPP2_TX10N	AE2
AD2	GPP2_RX9P	GPP2_TX9P	AC3
AD1	GPP2_RX9N	GPP2_TX9N	AC2
AB5	GPP2_RX8P	GPP2_TX8P	AB2
AB4	GPP2_RX8N	GPP2_TX8N	AB1
AA6	GPP2_RX7P	GPP2_TX7P	AA3
AA5	GPP2_RX7N	GPP2_TX7N	AA2
Y5	GPP2_RX6P	GPP2_TX6P	Y2
Y4	GPP2_RX6N	GPP2_TX6N	Y1
W6	GPP2_RX5P	GPP2_TX5P	W3
W5	GPP2_RX5N	GPP2_TX5N	W2
V5	GPP2_RX4P	GPP2_TX4P	V2
V4	GPP2_RX4N	GPP2_TX4N	V1
U6	GPP2_RX3P	GPP2_TX3P	U3
U5	GPP2_RX3N	GPP2_TX3N	U2
T5	GPP2_RX2P	GPP2_TX2P	T2
T4	GPP2_RX2N	GPP2_TX2N	T1
R6	GPP2_RX1P	GPP2_TX1P	R3
R5	GPP2_RX1N	GPP2_TX1N	R2
P5	GPP2_RX0P	GPP2_TX0P	P2
P4	GPP2_RX0N	GPP2_TX0N	P1

AD11	GPP3_RX9P	GPP3_TX9P	AH10
AC11	GPP3_RX9N	GPP3_TX9N	AG10
AE12	GPP3_RX8P	GPP3_TX8P	AG11
AD12	GPP3_RX8N	GPP3_TX8N	AE11
AC13	GPP3_RX7P	GPP3_TX7P	AH12
AE14	GPP3_RX7N	GPP3_TX7N	AG12
AD14	GPP3_RX6P	GPP3_TX6P	AG13
AD15	GPP3_RX6N	GPP3_TX6N	AE13
AC15	GPP3_RX5P	GPP3_TX5P	AH14
AE16	GPP3_RX5N	GPP3_TX5N	AG14
AD16	GPP3_RX4P	GPP3_TX4P	AG15
AD17	GPP3_RX4N	GPP3_TX4N	AF15
AC17	GPP3_RX3P	GPP3_TX3P	AH15
AE18	GPP3_RX3N	GPP3_TX3N	AG16
AD18	GPP3_RX2P	GPP3_TX2P	AG17
AD19	GPP3_RX2N	GPP3_TX2N	AE17
AC19	GPP3_RX1P	GPP3_TX1P	AH18
AH20	GPP3_RX1N	GPP3_TX1N	AG18
AG20	GPP3_RX0P	GPP3_TX0P	AG19
	GPP3_RX0N	GPP3_TX0N	AF19

AC21	SB_RX3P	SB_TX3P	AG22
AD21	SB_RX3N	SB_TX3N	AH22
AE22	SB_RX2P	SB_TX2P	AE21
AF25	SB_RX2N	SB_TX2N	AG21
AG25	SB_RX1P	SB_TX1P	AE23
AG26	SB_RX1N	SB_TX1N	AG23
AH26	SB_RX0P	SB_TX0P	AG24
	SB_RX0N	SB_TX0N	AH24

RX980/BGA892



PCI E slot TX need CAP close to slot side

GPP_TX5P_C	NC4	0.1u/4/X7R/16V/K	PCIE5_OP
GPP_TX5N_C	NC3	0.1u/4/X7R/16V/K	PCIE5_ON
GPP_TX4P_C	NC6	0.1u/4/X7R/16V/K	ML_OP
GPP_TX4N_C	NC5	0.1u/4/X7R/16V/K	ML_ON
GPP_TX2P_C	NC10	0.1u/4/X7R/16V/K	PCIE2_OP
GPP_TX2N_C	NC9	0.1u/4/X7R/16V/K	PCIE2_ON
GPP_TX1P_C	NC20	0.1u/4/X7R/16V/K	PCIE1_OP
GPP_TX1N_C	NC19	0.1u/4/X7R/16V/K	PCIE1_ON
GPP_TX0P_C	NC2	0.1u/4/X7R/16V/K	USB3_OP
GPP_TX0N_C	NC1	0.1u/4/X7R/16V/K	USB3_ON

A_TX3P_C	NC11	0.1u/4/X7R/16V/K	A_TX3P
A_TX3N_C	NC12	0.1u/4/X7R/16V/K	A_TX3N
A_TX2P_C	NC14	0.1u/4/X7R/16V/K	A_TX2P
A_TX2N_C	NC13	0.1u/4/X7R/16V/K	A_TX2N
A_TX1P_C	NC15	0.1u/4/X7R/16V/K	A_TX1P
A_TX1N_C	NC16	0.1u/4/X7R/16V/K	A_TX1N
A_TX0P_C	NC18	0.1u/4/X7R/16V/K	A_TX0P
A_TX0N_C	NC17	0.1u/4/X7R/16V/K	A_TX0N

PLACE THESE CAP CLOSE TO NB.

EXP\_A\_TXP0\_15I &gt;&gt;&gt; EXP\_A\_TXP[0..15] 18

EXP\_A\_TXN0\_15I &gt;&gt;&gt; EXP\_A\_TXN[0..15] 18

EXP\_A\_RXP0\_15I &gt;&gt;&gt; EXP\_A\_RXP[0..15] 18

EXP\_A\_RXN0\_15I &gt;&gt;&gt; EXP\_A\_RXN[0..15] 18

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Title  
RS780 PCIE I/F\_SwitchSize  
Custom Document Number  
GA-970A-D3

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Rev  
1.02



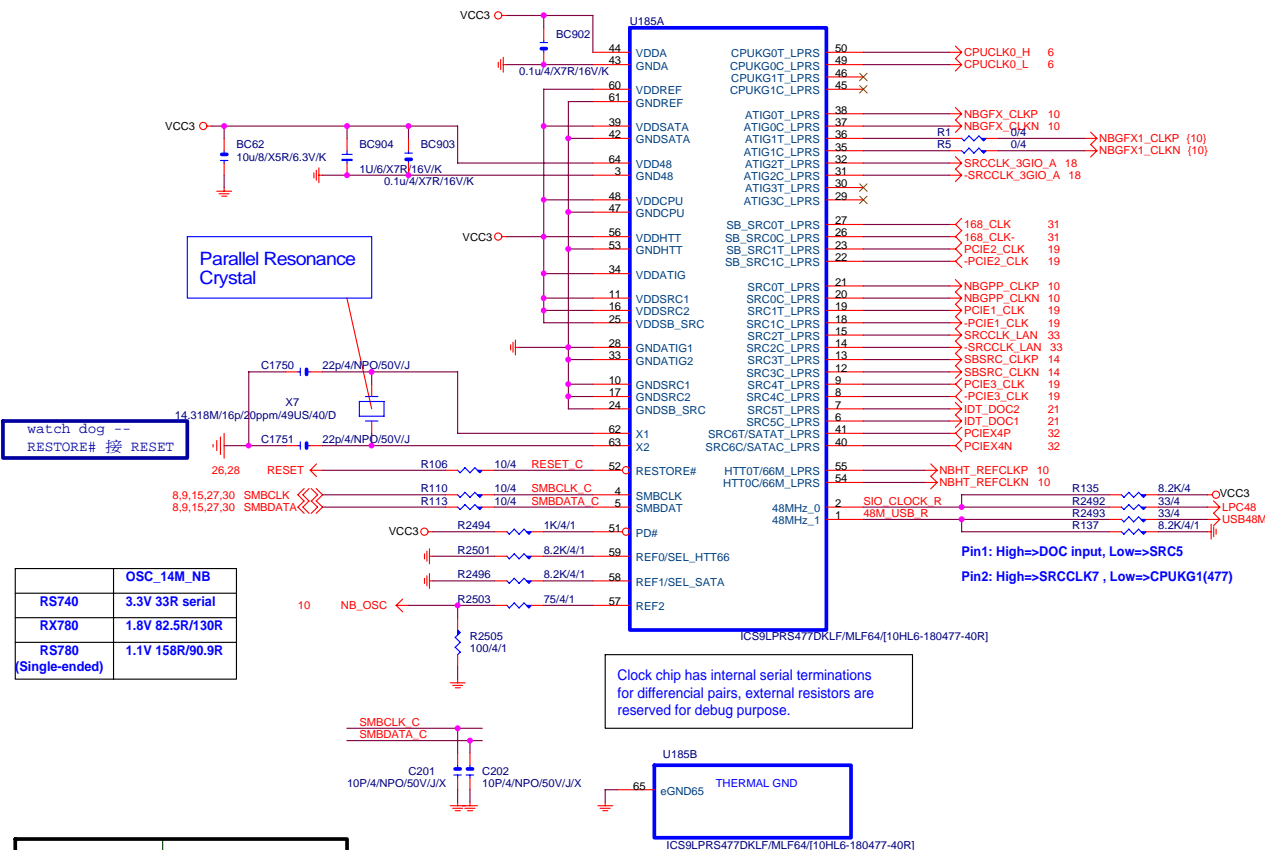
## NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mills away from U800  
R851 less than 100 mills away from R800/801  
route CPU clock as 100ohm differential pair



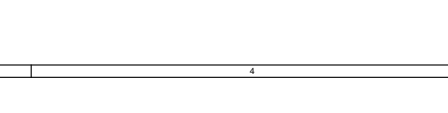
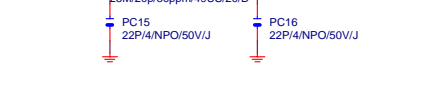
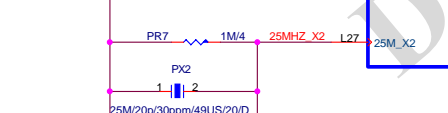
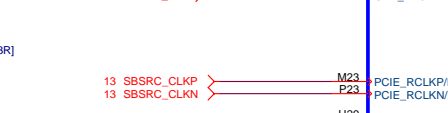
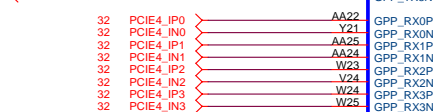
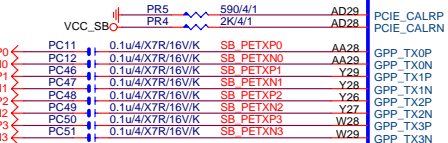
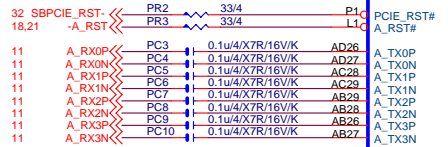
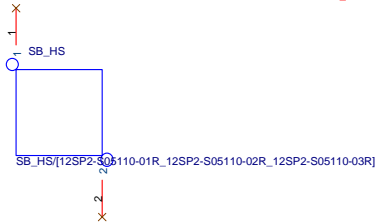
GIGABYTE™

Title			RTM880N-793		
Size	Document Number	GA-970A-D3			Rev
Custom					1.02
Date:	Tuesday, June 28, 2011	Sheet	13	of	36



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK



SB850

Part 1 of 5

PCIE CLKs

PCIE EXPRESS INTERFACES

PCIE INTERFACE

CLOCK GENERATOR

CPU

RTC

INTRUDER ALERT

VDDBT\_RTC\_G

SB950/BGA605/[10HB1-06B950-10R]

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

PCIE\_RST#

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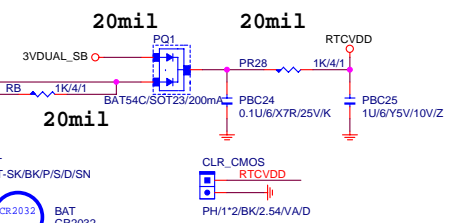
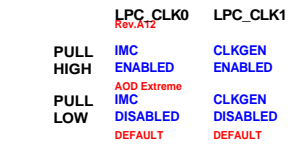
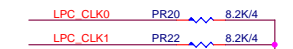
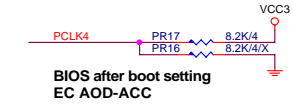
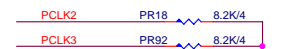
PCIE\_RST#

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PCIE\_RST#

Low: Force PCIE GEN1, Up: Allow PCIE GEN2



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

**GIGABYTE**

ATI SB700 PCIE/PCI/CPU/LPC

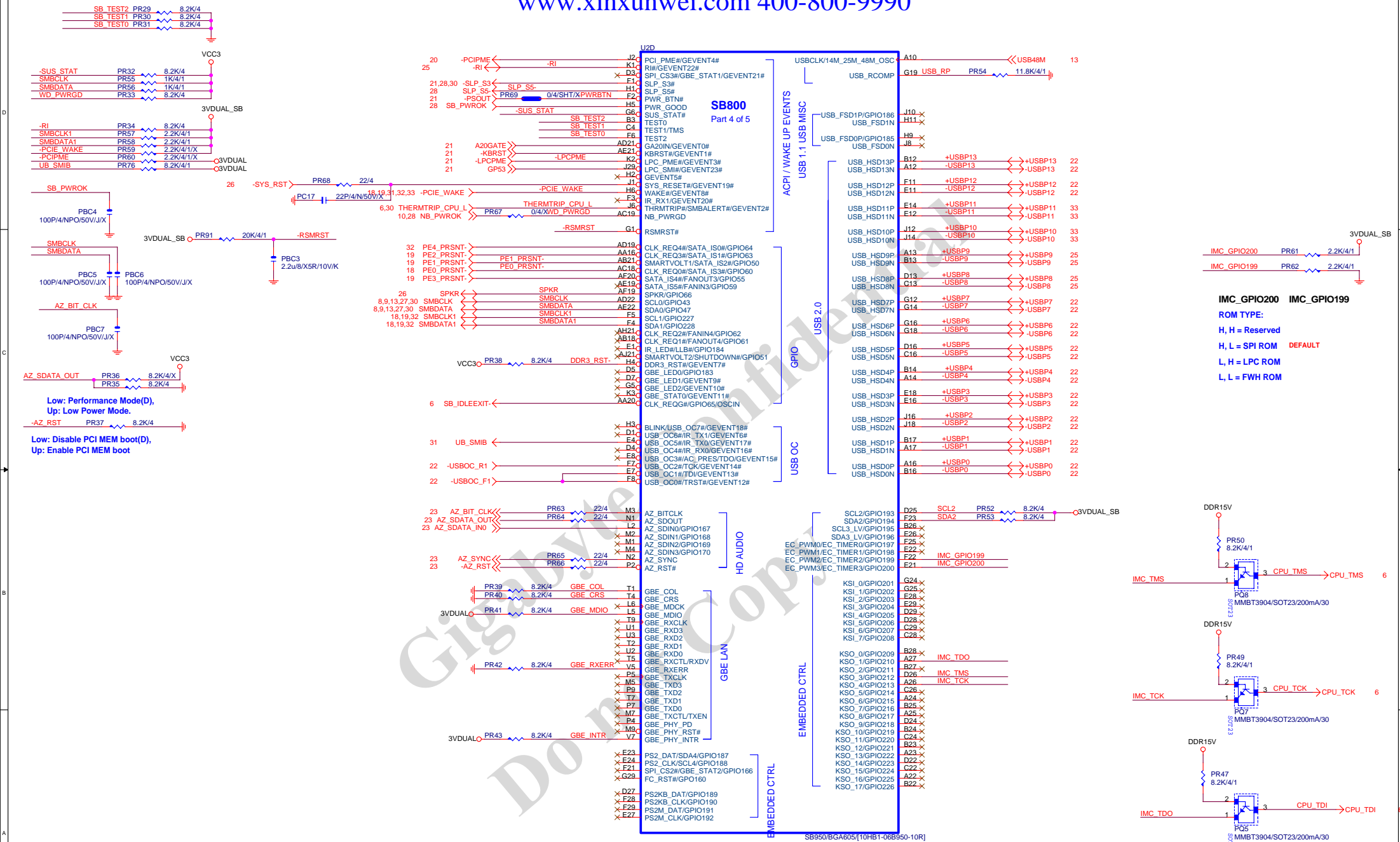
Rev. 1.02

GA-970A-D3

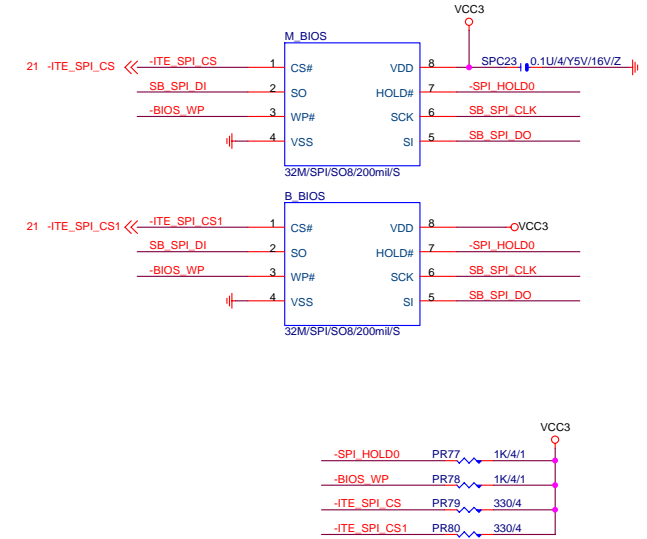
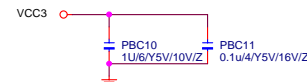
Tuesday, June 28, 2011

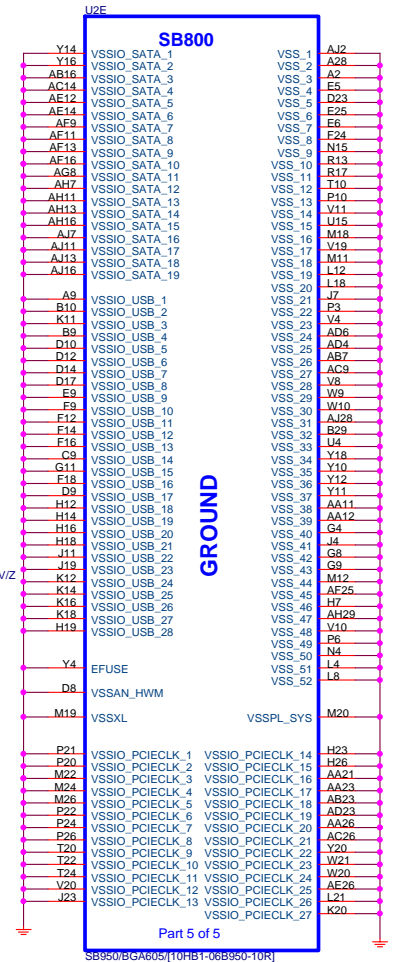
Sheet 14 of 36

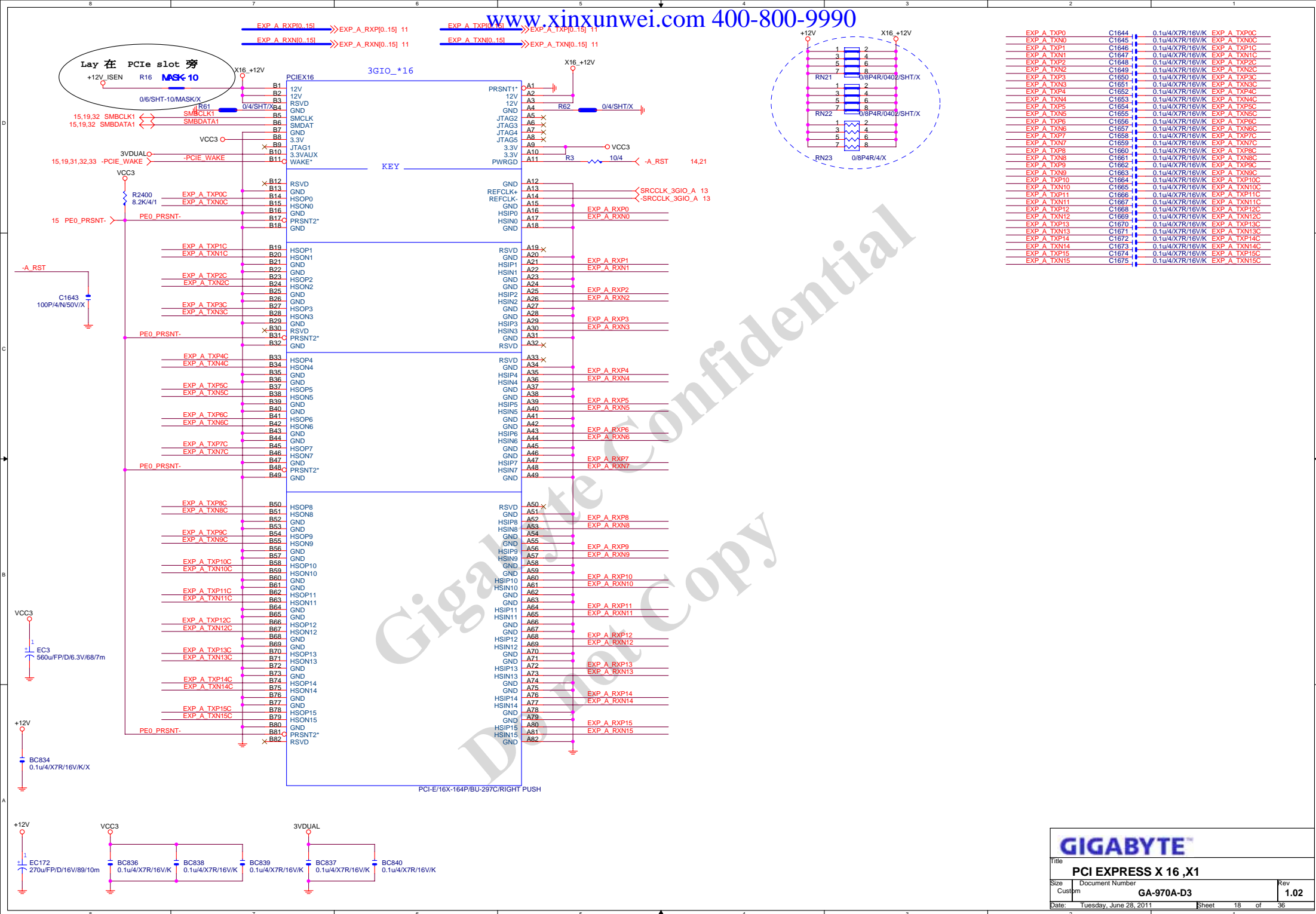


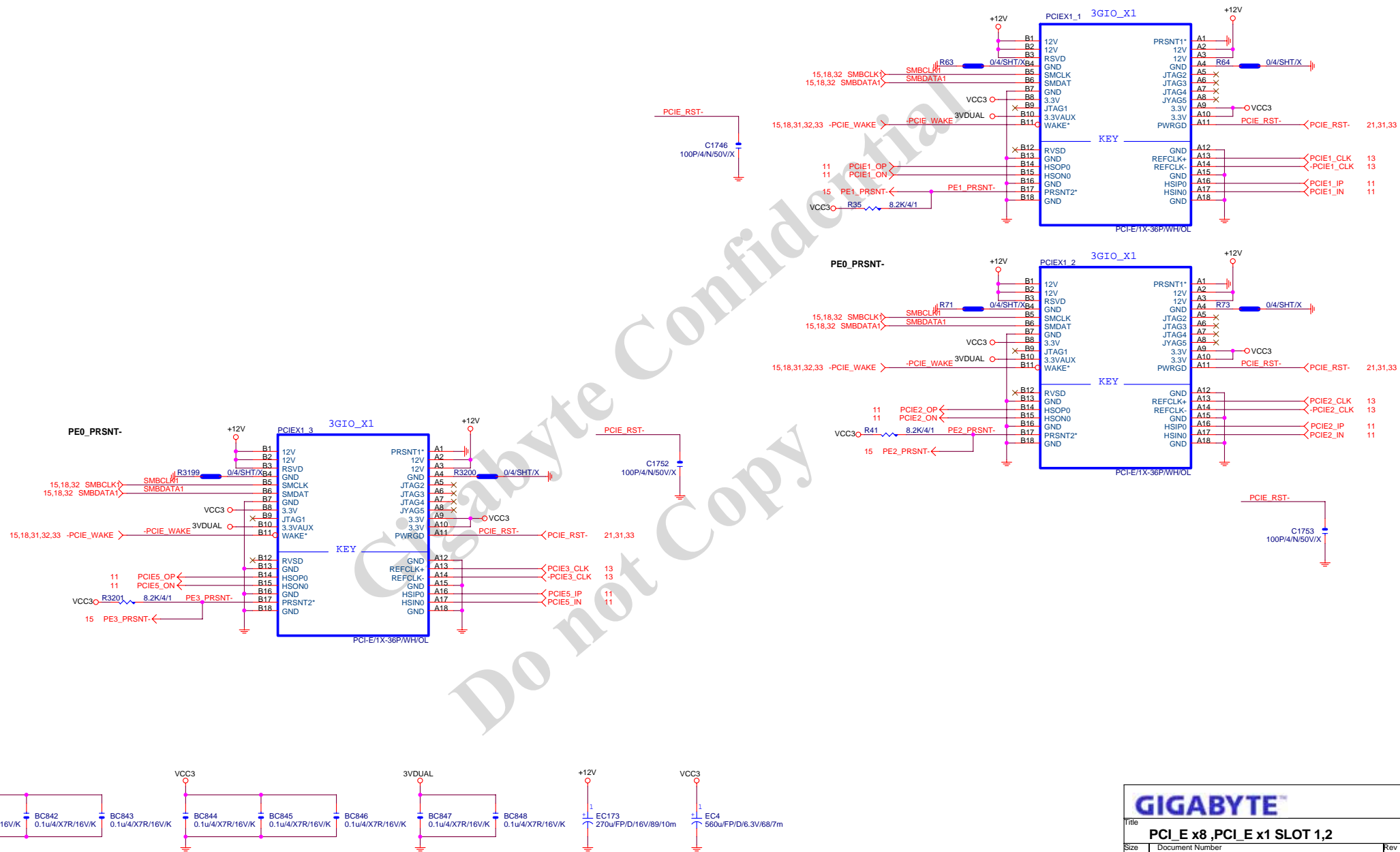


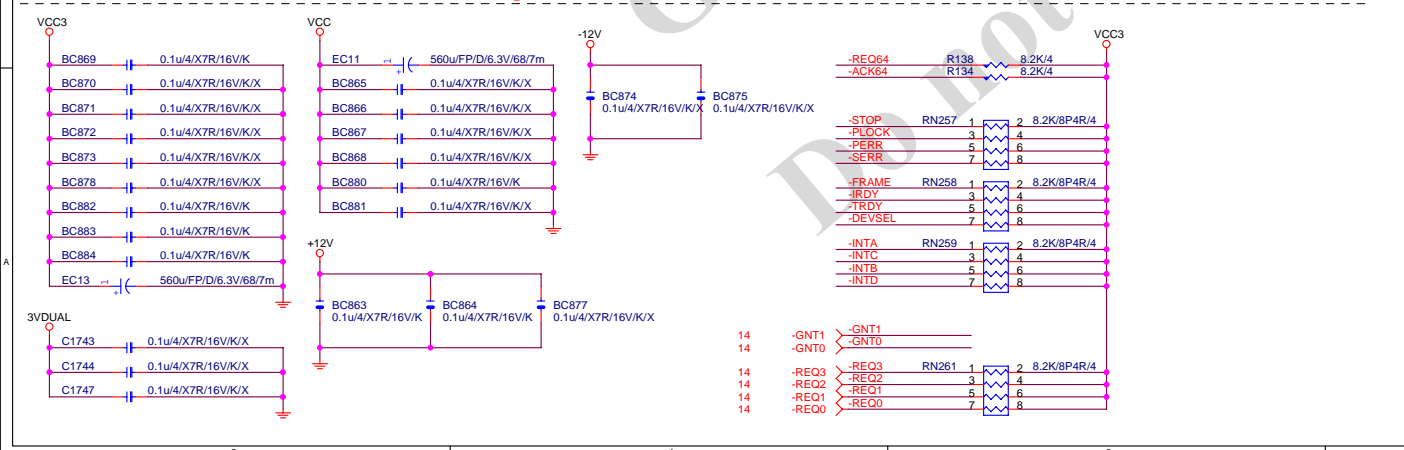


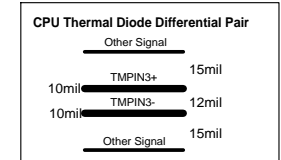


[illegible]










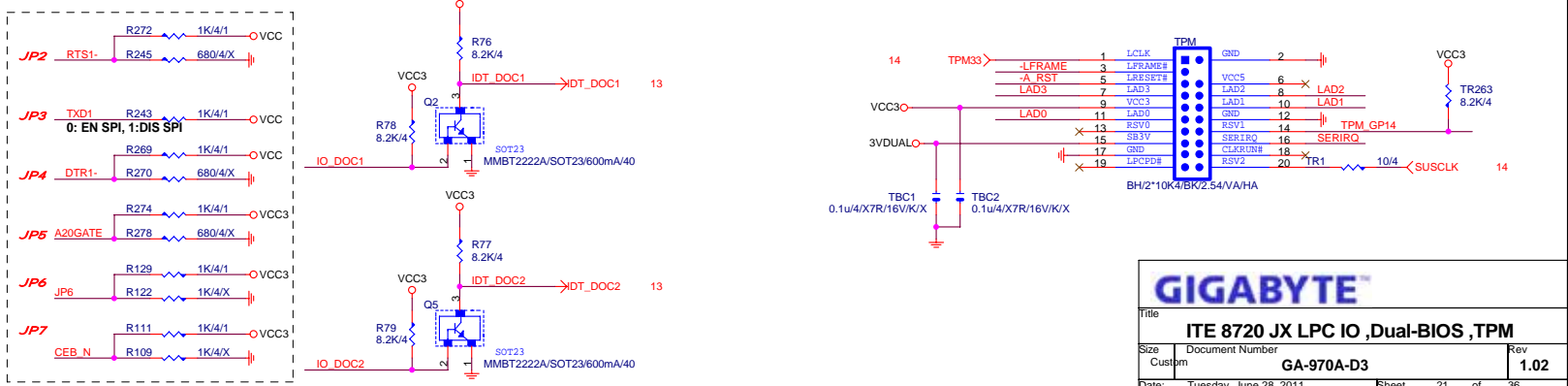
IT8720F ( GB )

**ITE COMMENTS**

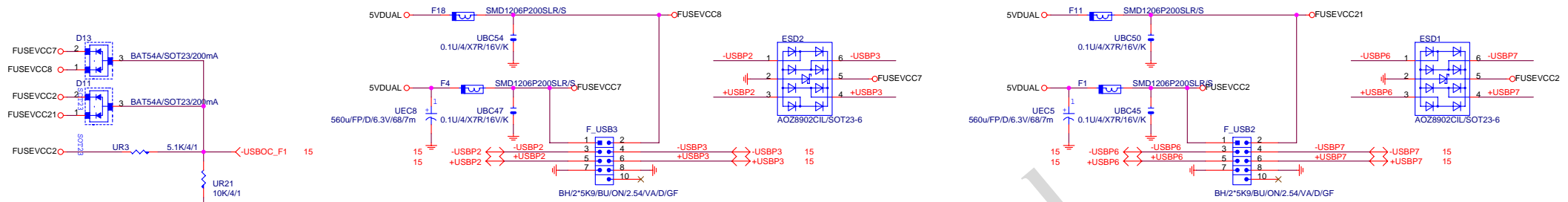
26 COPEN-

Dual BIOS Reset change to KBRST: because pin 109 is AND of (1.VCC, 2.ATXPWROK, 3.SLP\_S3-, 4.RESETCON-), but when G3 to S5, pin 79 will pass to pin 61. But pin 79 is unknown when G3 to S5, when pin 79 high, boot ok, but when pin79 is low it will hang a "FF." Because pin 109 will cause system reset low.

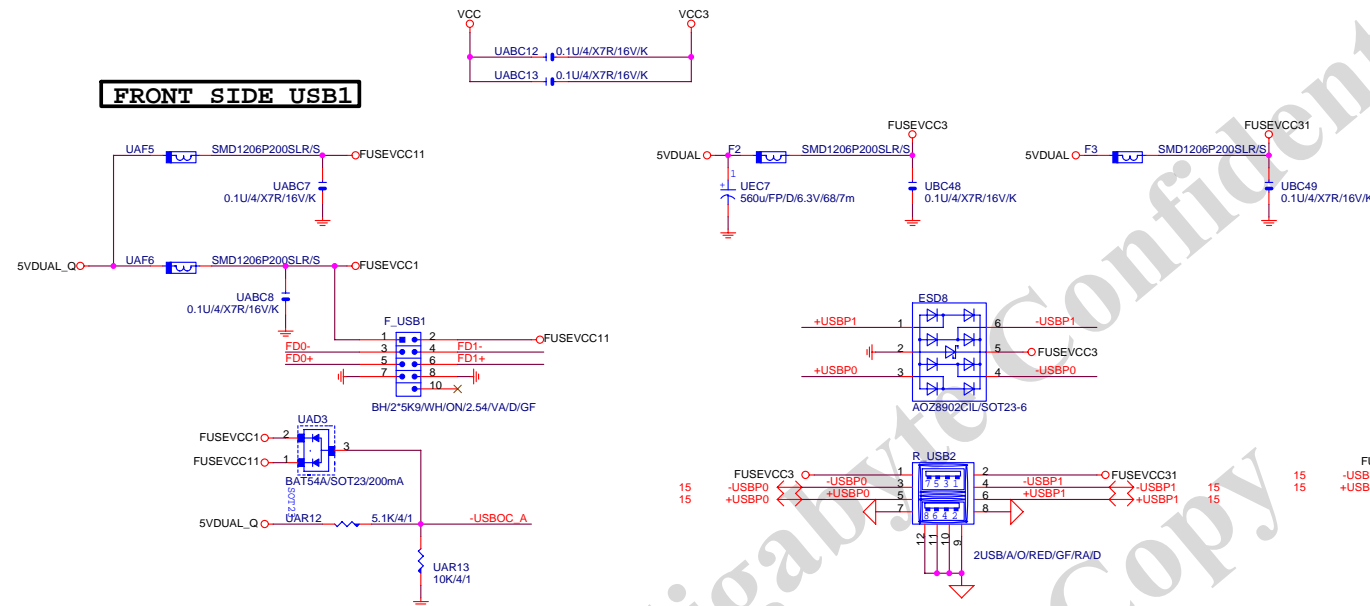
	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only



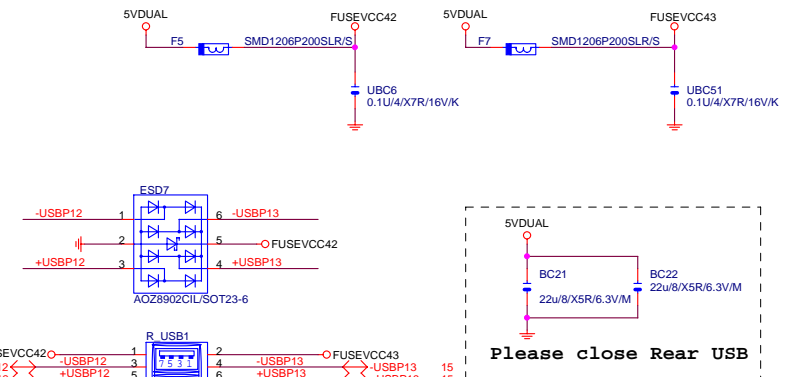




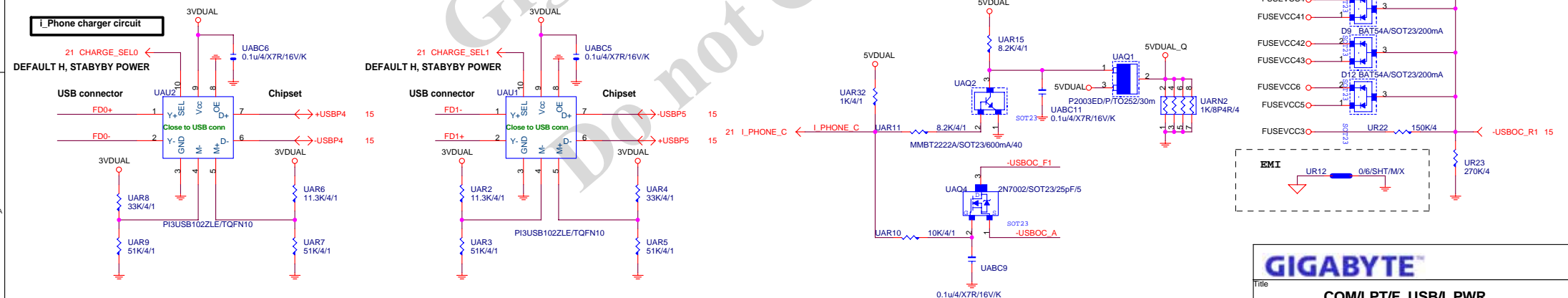
## FRONT SIDE USB1



## REAR USB



## I-Phone charger circuit



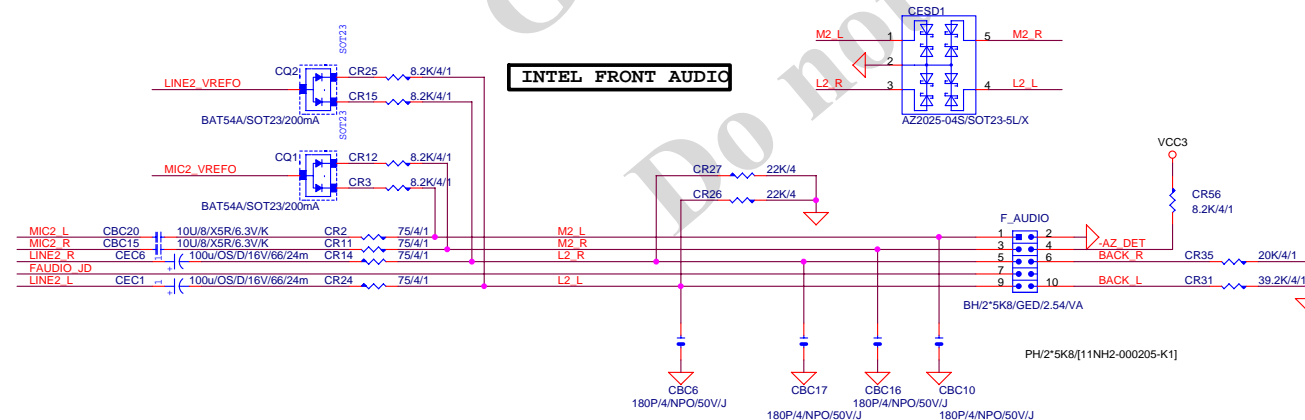
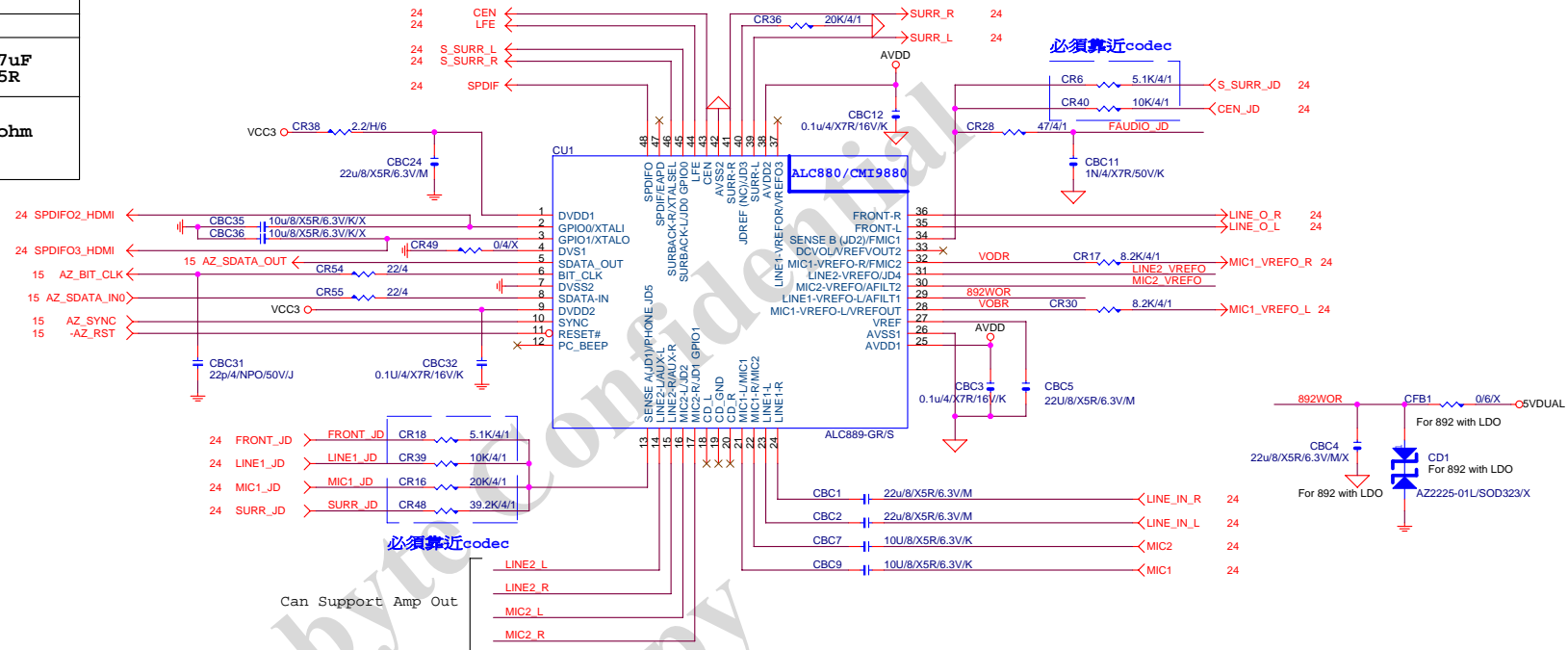
GIGABYTE

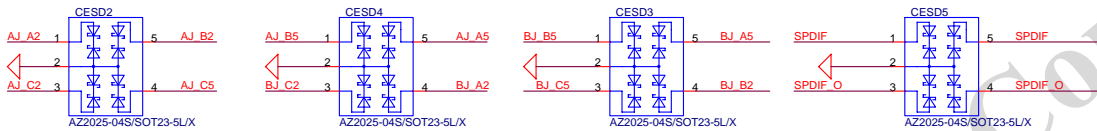
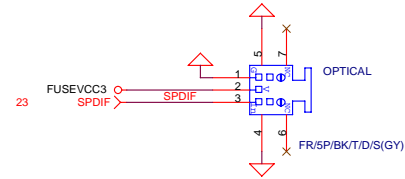
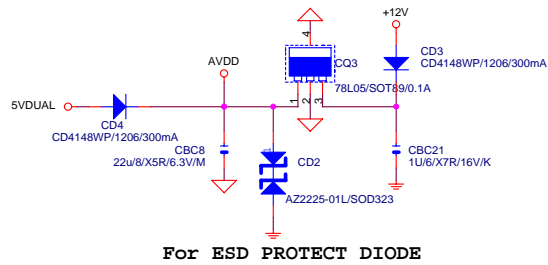
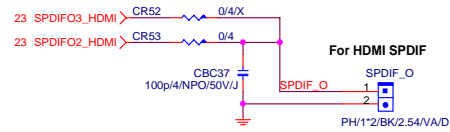
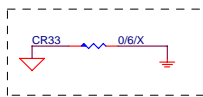
COM/LPT/F\_USB/I\_PWR

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Date:	Tuesday, June 28, 2011	Sheet 22 of 36

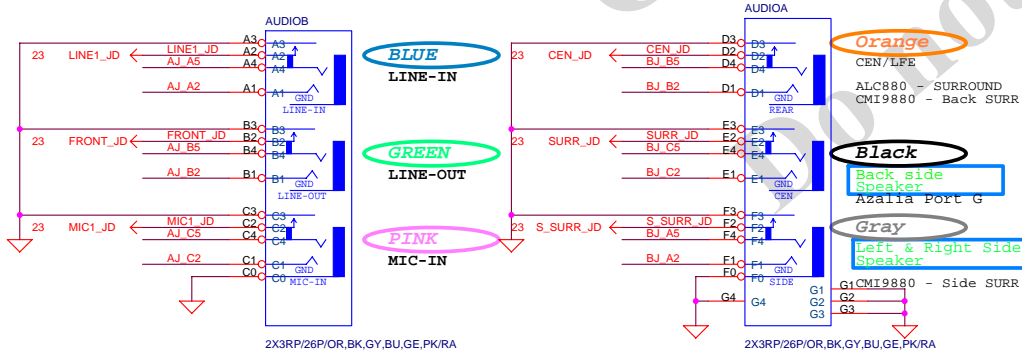
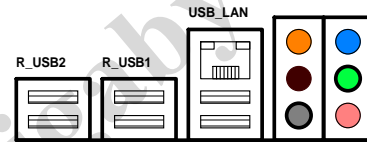
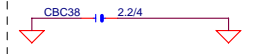


	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm





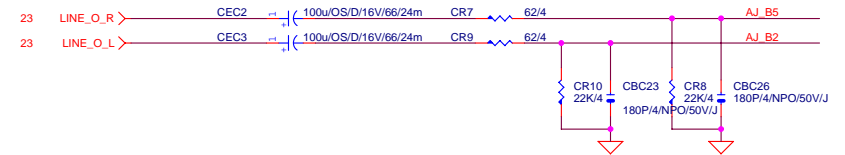
For Audio precision test



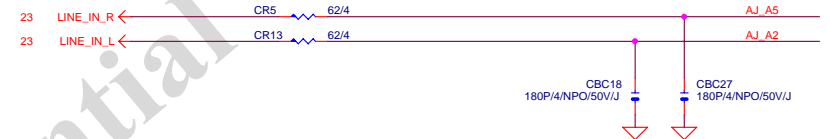
A3R7/13P/B/[11NR6-403006-01\_11NR6-403006-02]  
3R7+15P/[11NR6-403004-11]

A3R7/13P/0BG/[11NR6-403006-71]  
3R7+15P/[11NR6-403004-31]

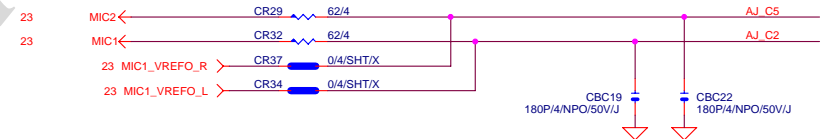
### LINE OUT FRONT OUT



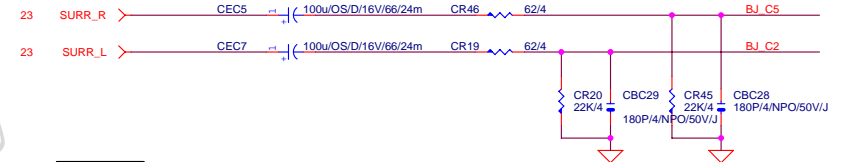
### LINE-IN



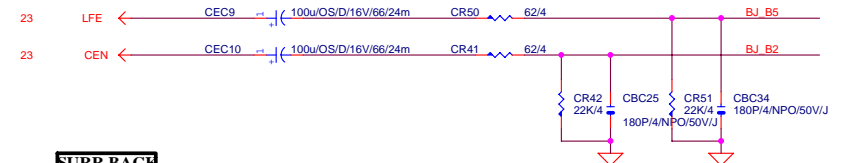
### MIC



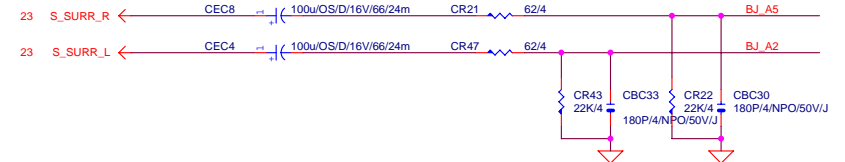
### SURROUND



### CEN/LFE



### SURR BACK



**GIGABYTE**

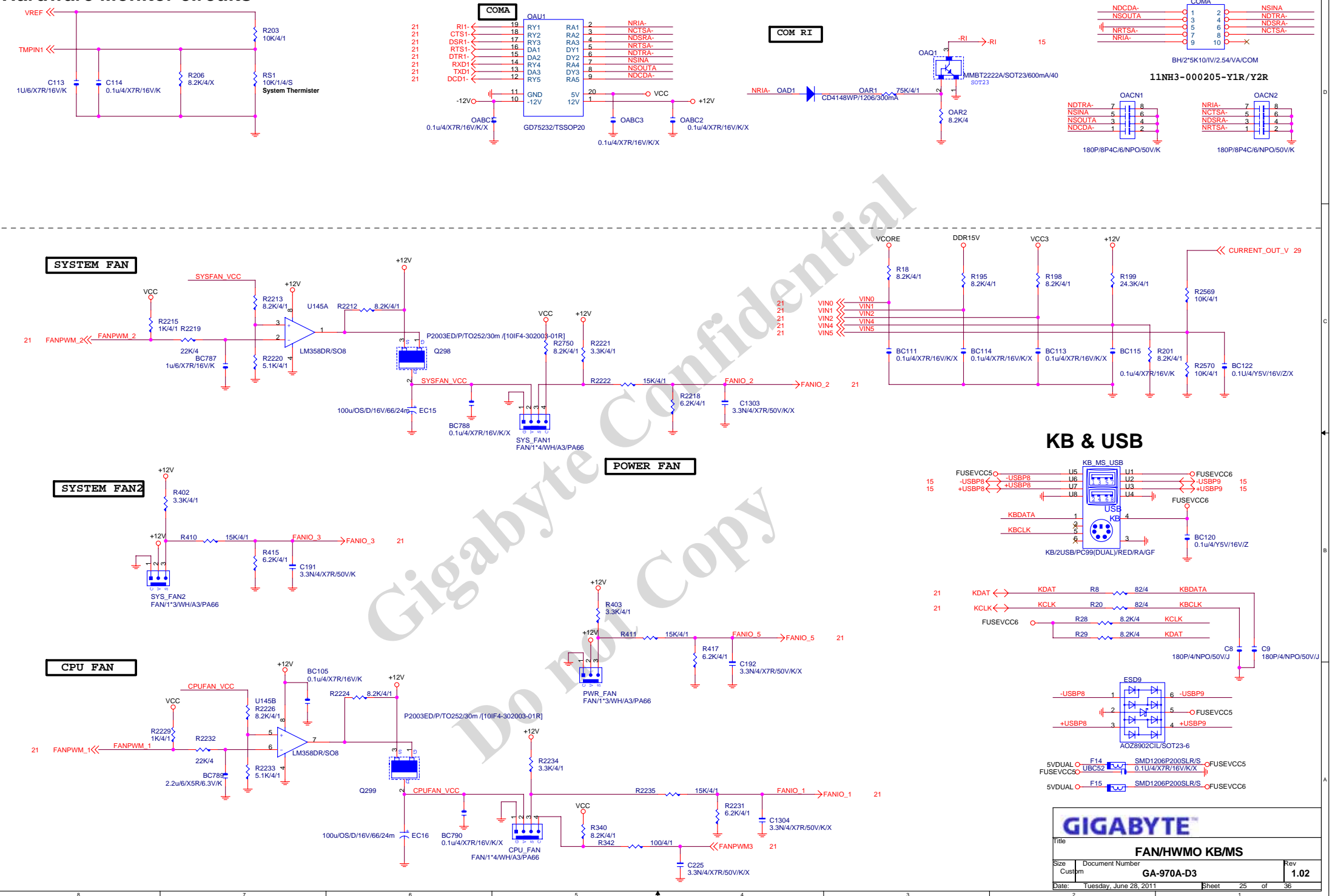
Title  
**AUDIO JACK**

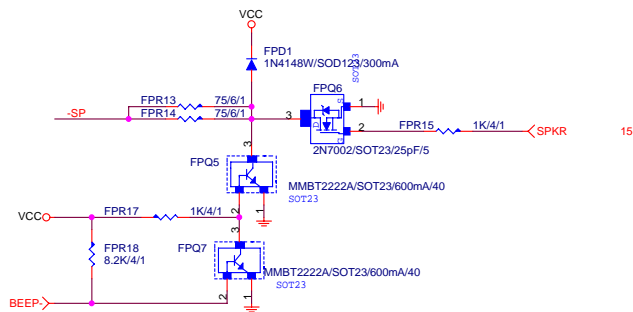
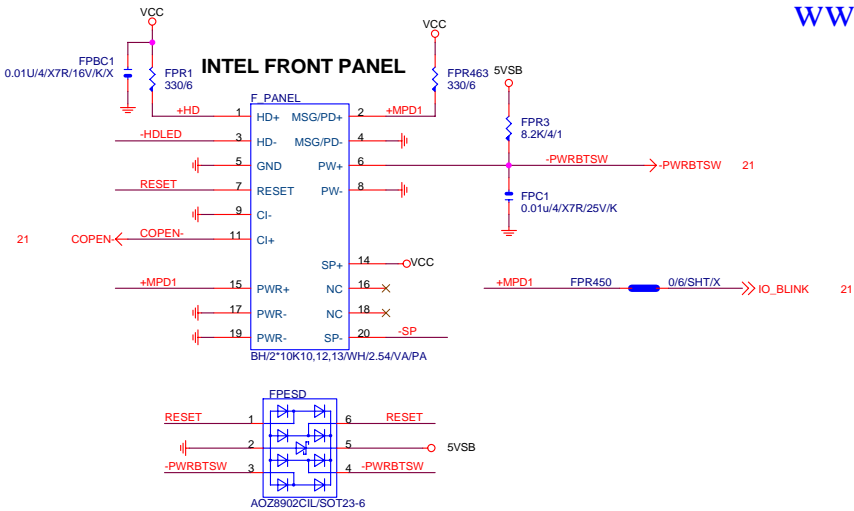
Size Document Number  
Custom **GA-970A-D3**

Rev  
**1.02**

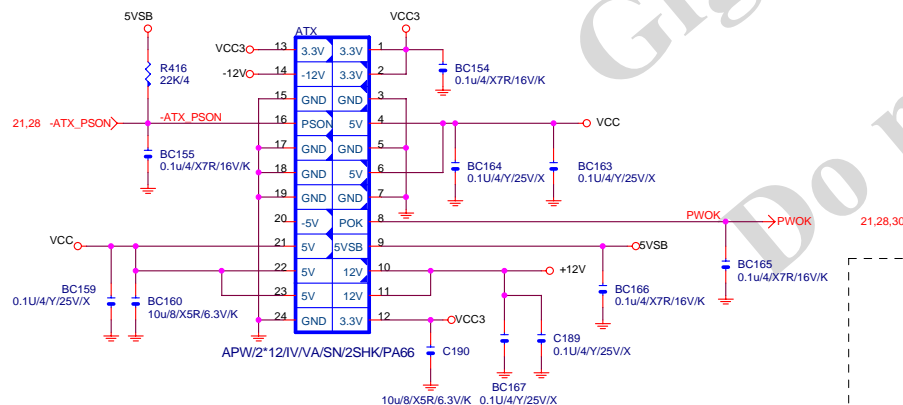
Date: Tuesday, June 28, 2011 Sheet 24 of 36

Hardware Monitor circuits

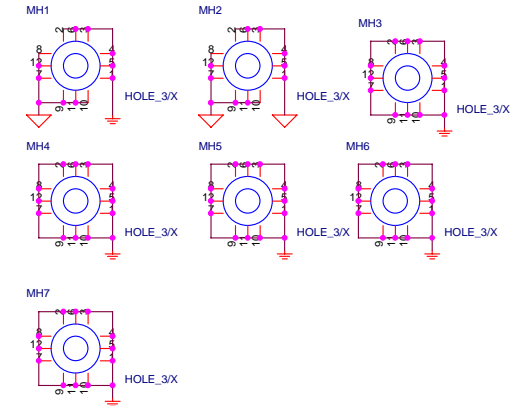
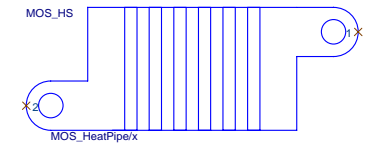
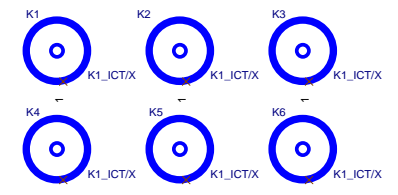
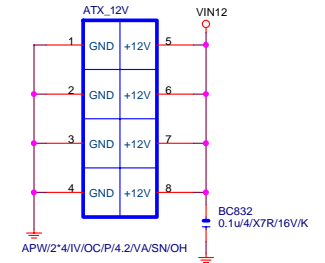
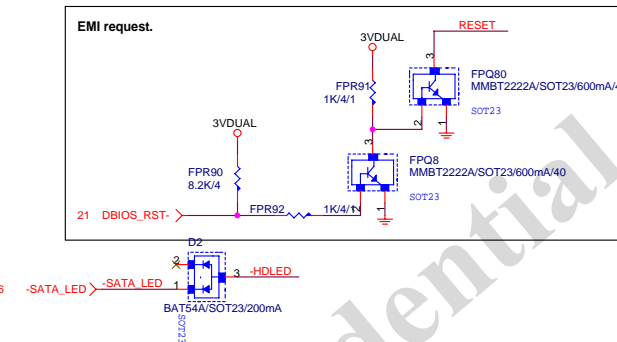




### ATX POWER CONNECTOR

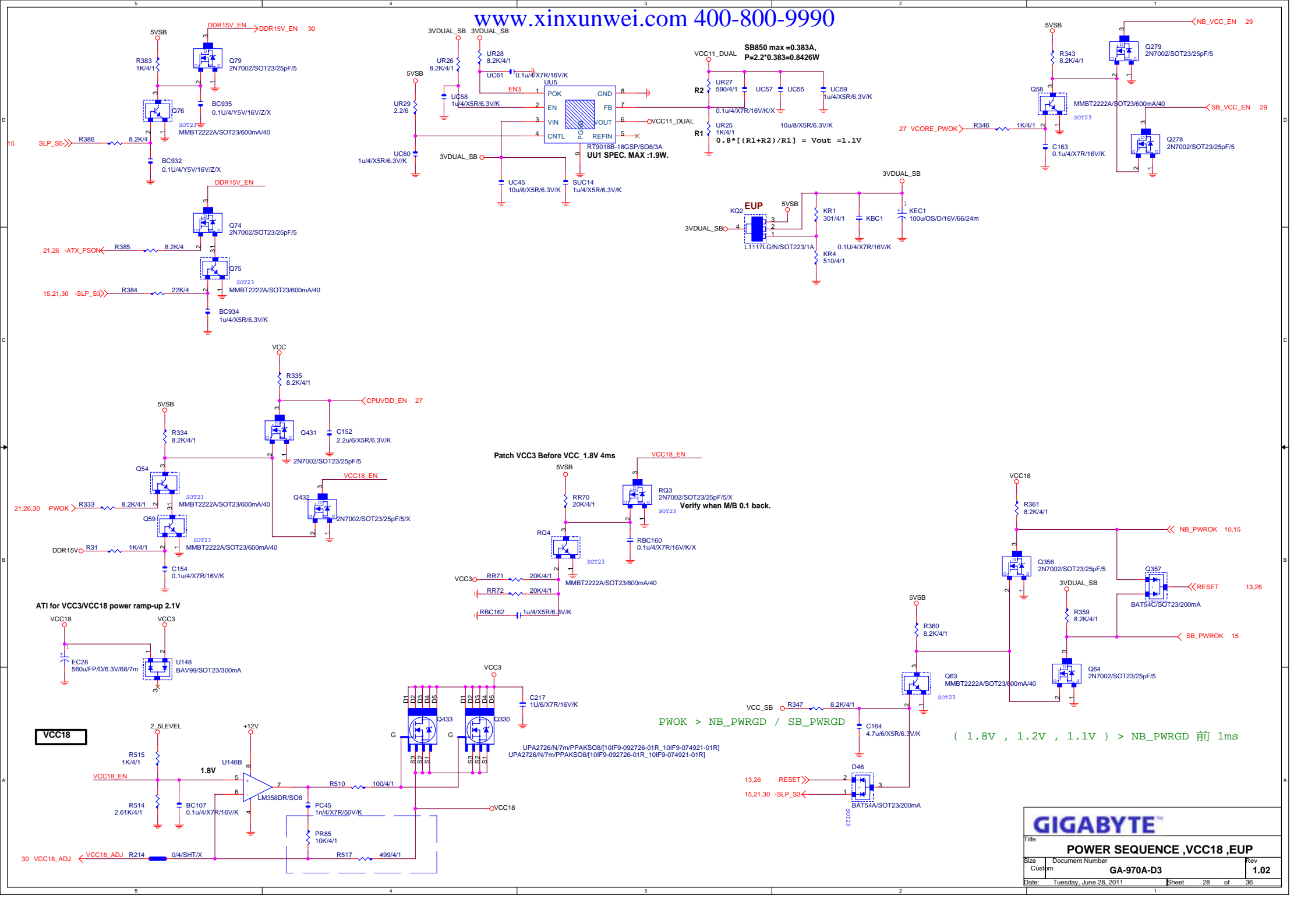


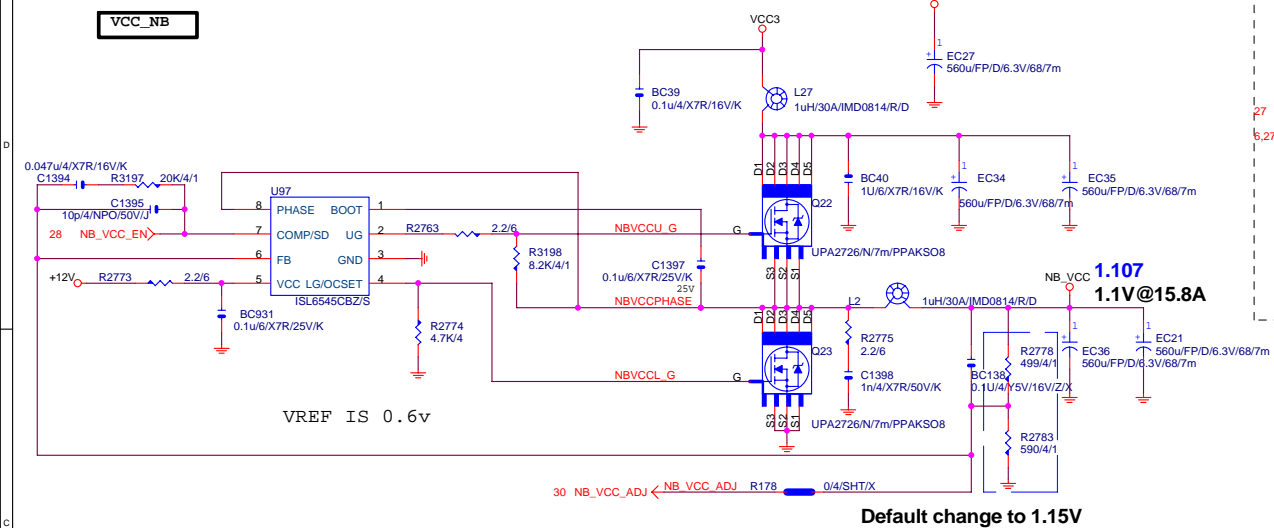
For Seasonic 900W  
Power supply  
cant Boot issue



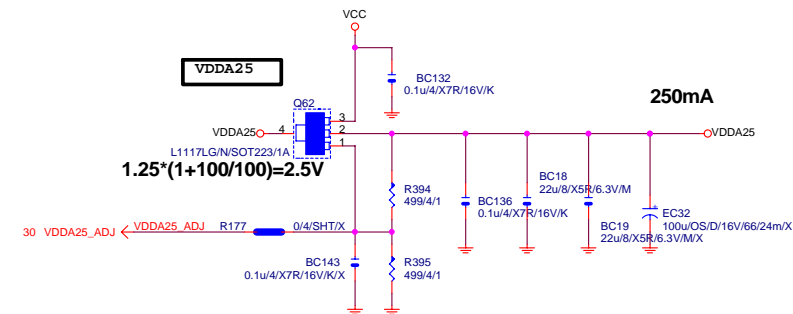
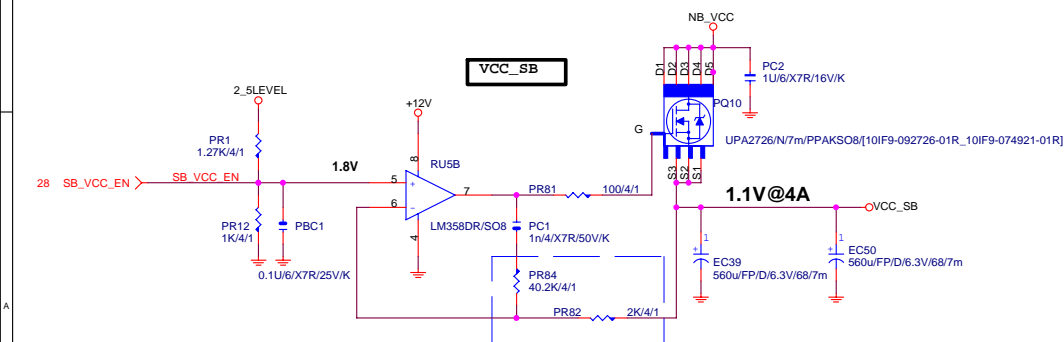
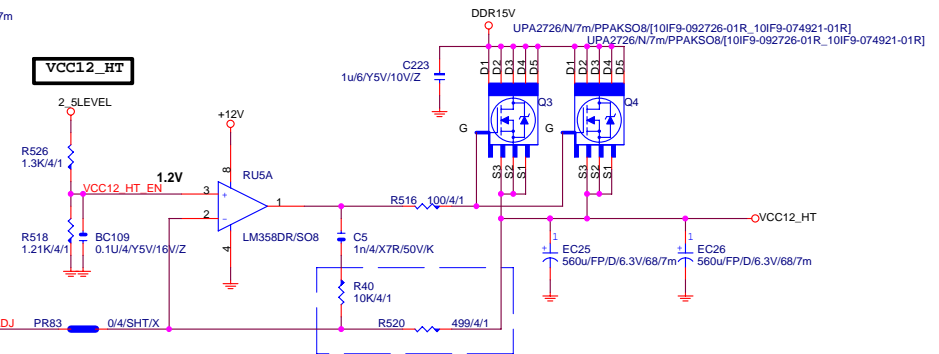
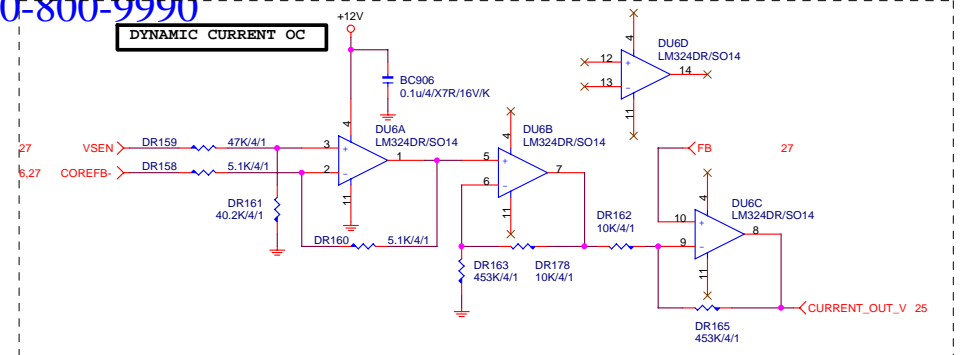
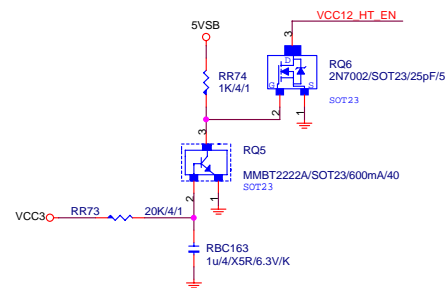
GIGABYTE			
Title			
ATX, FRONT PANEL ,EC			
Size	Document Number	Rev	
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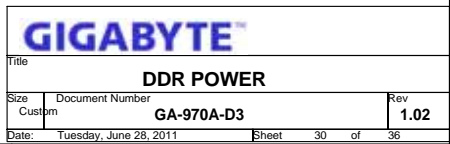


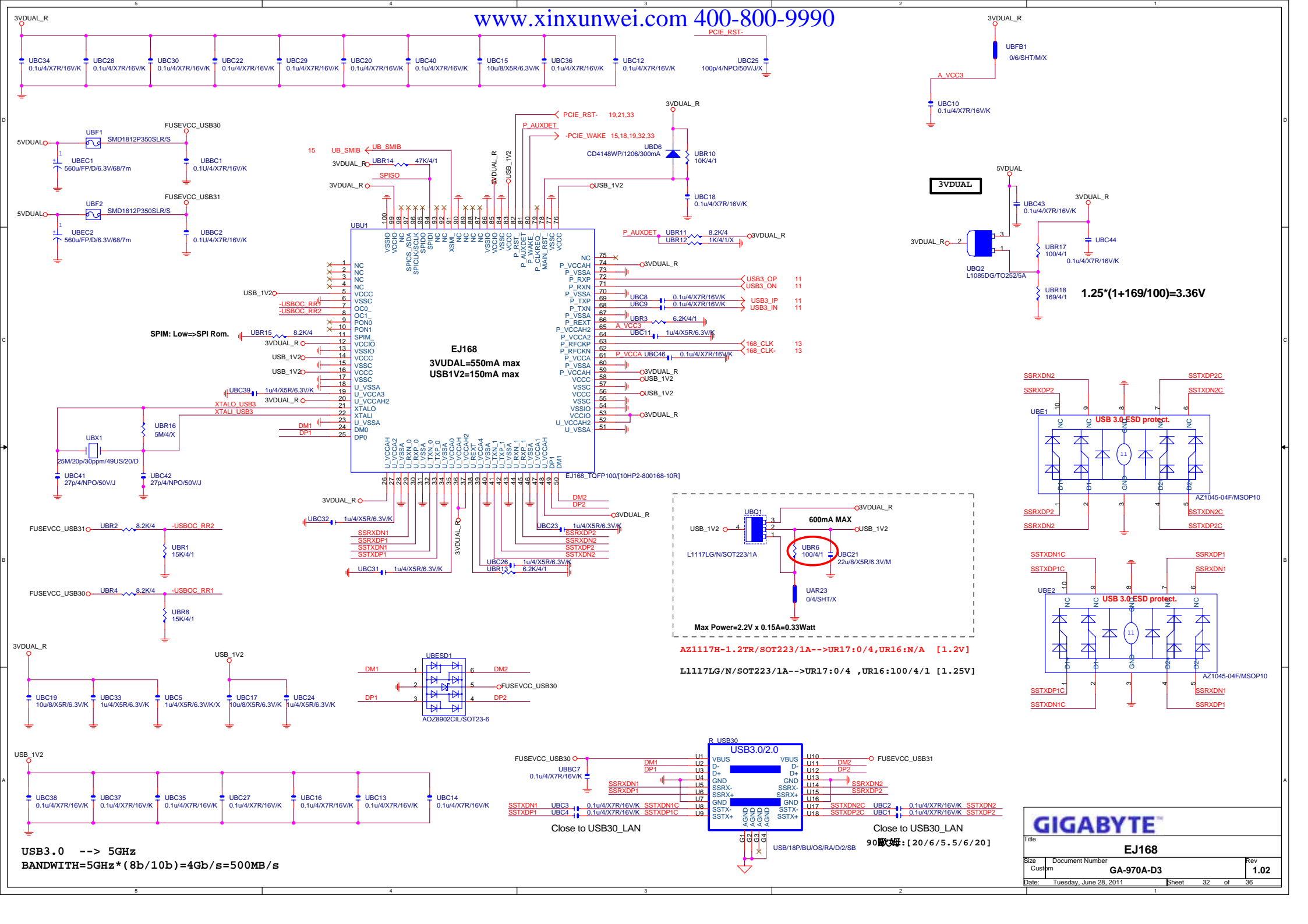


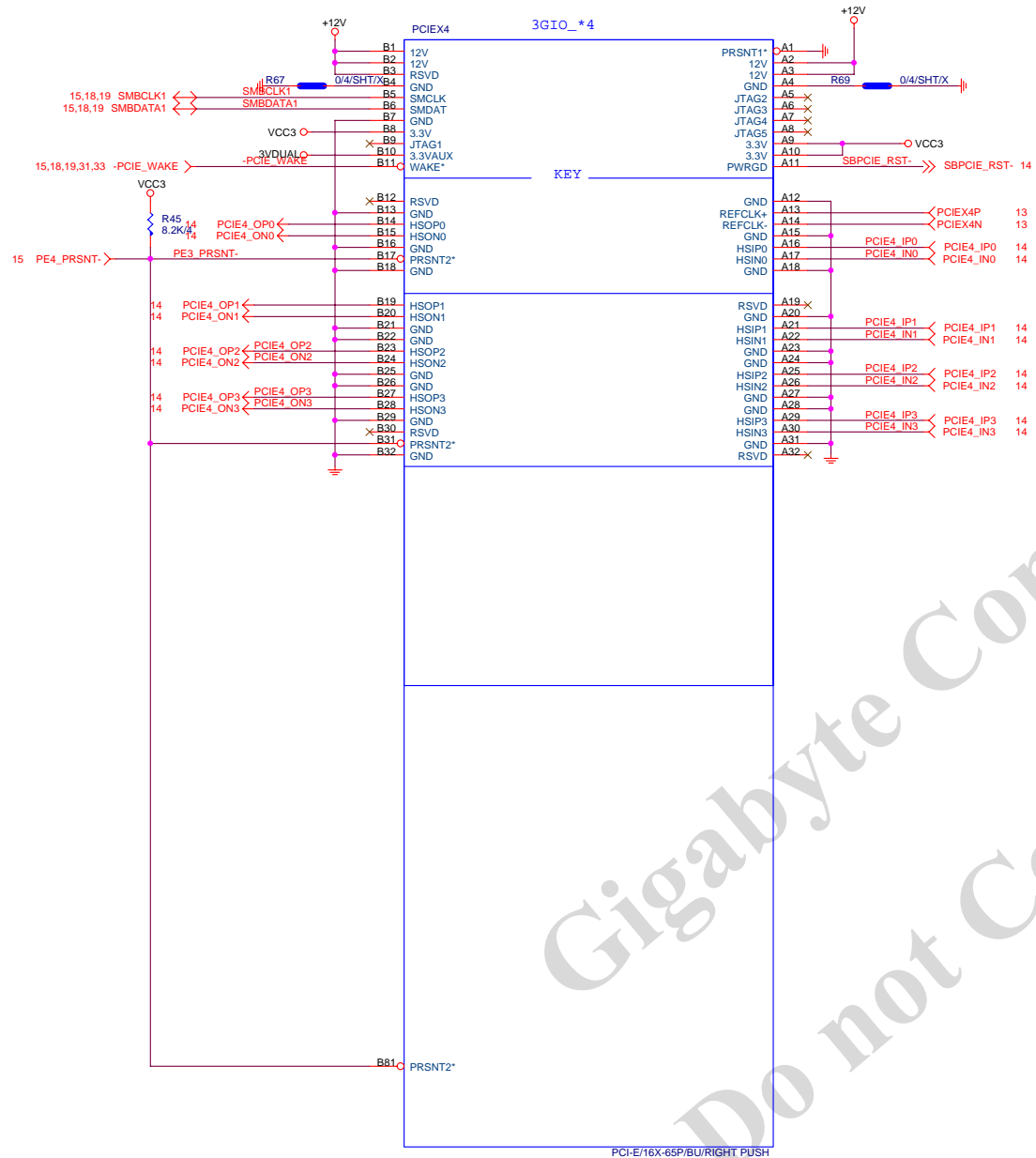
## Patch AMD Validation VDDA25 & VCC12\_HT power sequence









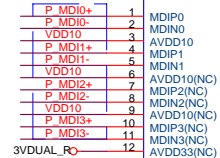


**GIGABYTE™**

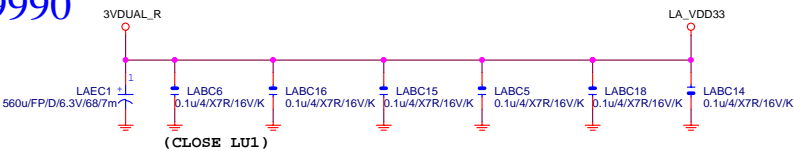
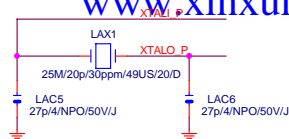
Title			
JMB362			
Size	Document Number	Rev	
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要用1% 的電阻,trace不能太長,建議在200 mil以內

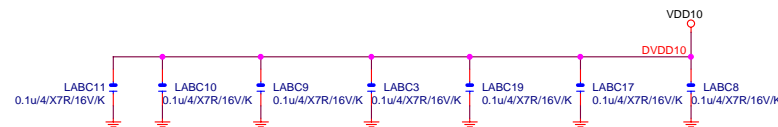
要用1% 的電阻,trace不能太長,建議在200 mil以內



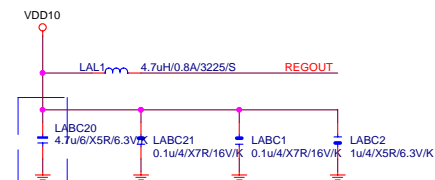
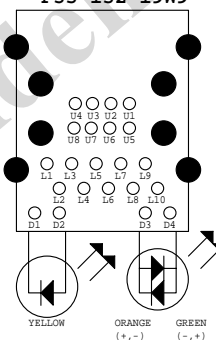
Pin34/35(VDDREG) 接到3VDUAL  
的trace 建議寬度大於 40mil



(CLOSE LU1)



P35-152-19W9

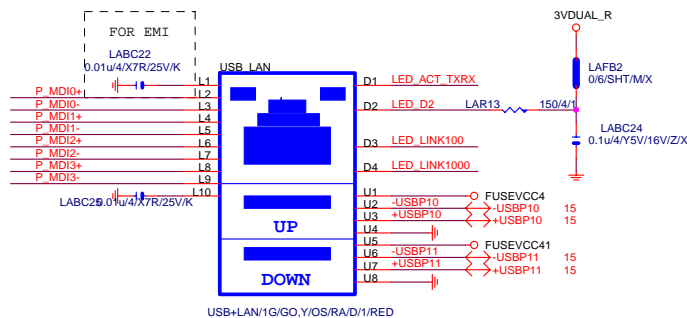


建議使用X5R電容

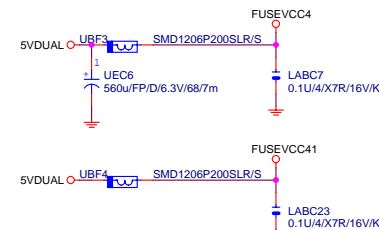
## RTL8101E:LR38/LC5/LR43/LC6--&gt;0

```
RTL8111C:LC6-->0
```

RTL8102E:LC5/LC6--&gt;0

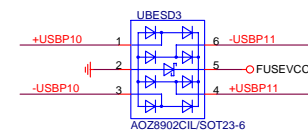
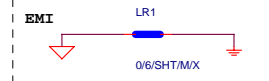


USB+LAN/1G/GO,Y/OS/RA/D/1/RED



```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

```
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```

**GIGABYTE™**

REALTK RTL8111C

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